

## Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells<sup>1</sup> and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent  $1\mu m$  to smaller structure sizes. **This process is for manufacturing  $1\mu m$  only!** But further releases which will have been tested with smaller structure sizes can be expected.

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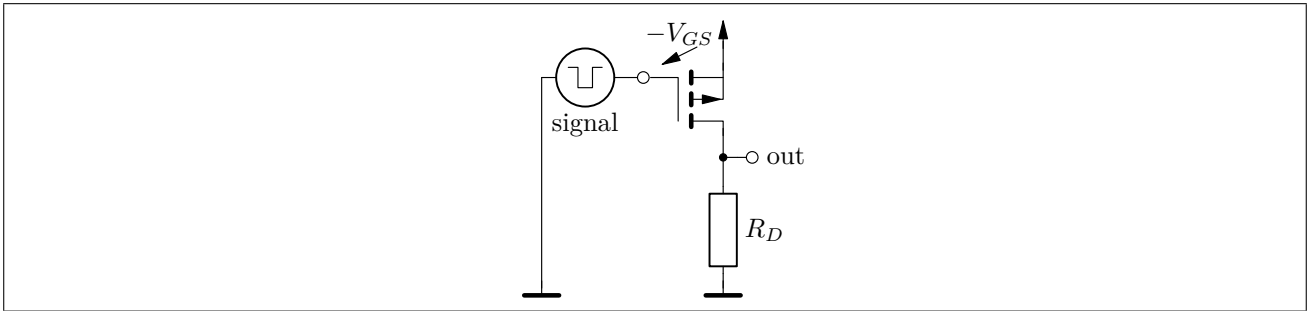
<sup>1</sup><https://github.com/chipforge/StdCellLib>

# CMOS in a nutshell

Hagen Sankowski

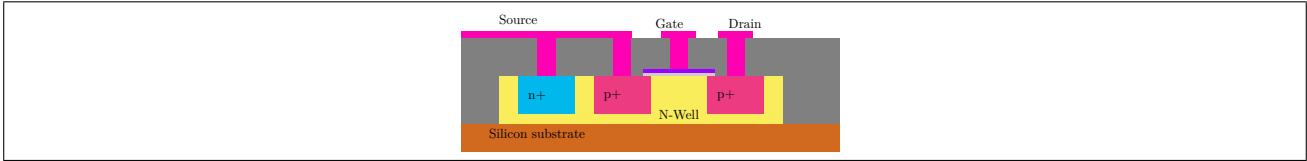
June 3, 2018

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal-oxide-semiconductor field-effect transistors (MOSFET) are required. Historically, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.



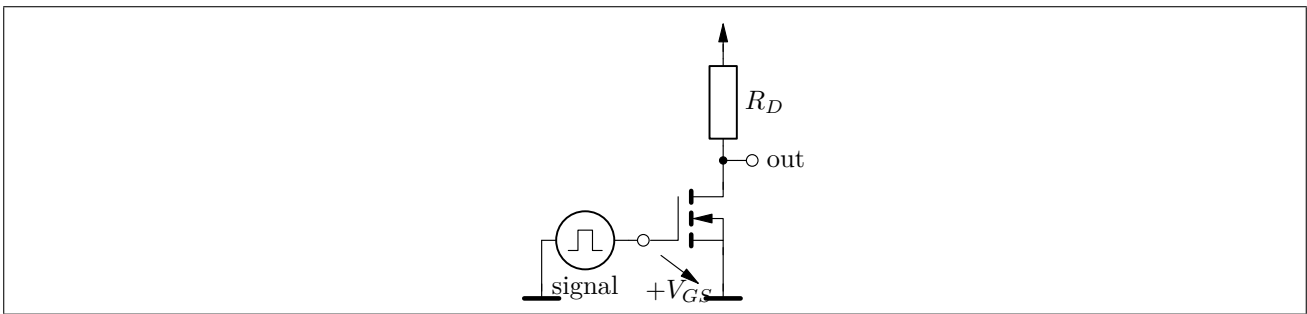
**Figure 1:** enhancement-mode PMOS transistor use-case

The sectional view of a PMOS transistor in silicon is shown below



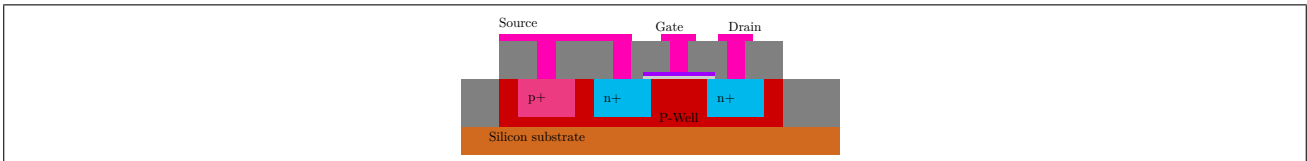
**Figure 2:** Sectional view of a PMOS transistor

Historically later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.



**Figure 3:** enhancement-mode NMOS transistor use-case

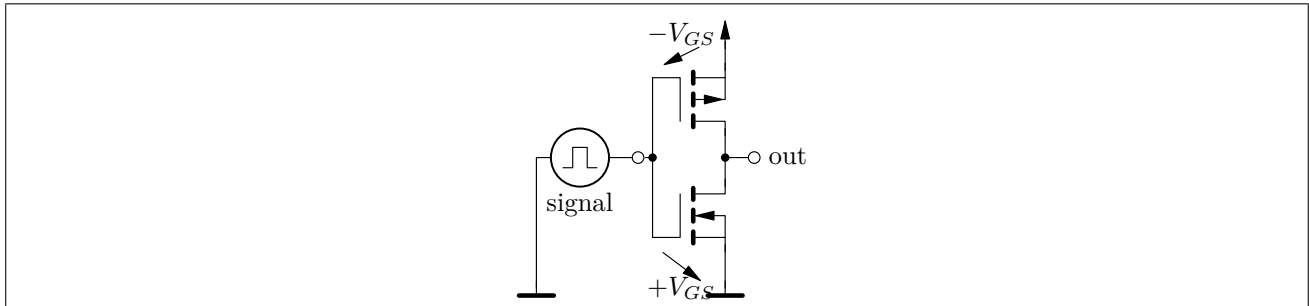
The sectional view of a NMOS transistor in silicon is shown here also.



**Figure 4:** Sectional view of a NMOS transistor

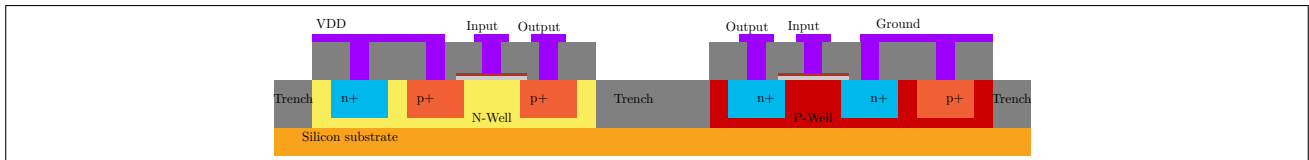
Both technologies, the older PMOS as the newer NMOS, have the same disadvantage. Every time, the transistor is switched on, the current between drain and source of the transistor is limited by the resistor on drain only.

Higher currents here means higher power consumption for the chip where the transistors are integrated as well. If the transistors are switched off, no current flows between drain and source anymore, the power consumption of the chip also goes low. Et violá, the US-Patent with Number 3356858<sup>1</sup> changed the world and combines both technologies to the new complementary metal-oxide-semiconductor (CMOS) technology. Instead of every transistor working against a weak resistor, the transistor works against a complementary switched-off transistor. With the eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are built in CMOS.



**Figure 5:** complementary PMOS and NMOS transistor couple use-case

Below the sectional view of the inverter circuitry can be seen. For the run through of this process we will use this cross section diagram as reference.



**Figure 6:** Sectional view of a NMOS-PMOS transistor circuit

<sup>1</sup><https://www.google.com/patents/US3356858>