

Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells¹ and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

¹<https://github.com/chipforge/StdCellLib>

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Physics essentials for LibreSilicon

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In this document we deal with all the physics related to solid state device manufacturing. In case there is anything unclear, please look up this document and its chapters.

1 Getting doping from resistance

In many cases the supplier will only provide the resistance per length specification for their substrate and won't give you the dopant concentration numbers. In this case you will have to find these numbers out yourself by converting it from the numbers they've provided.

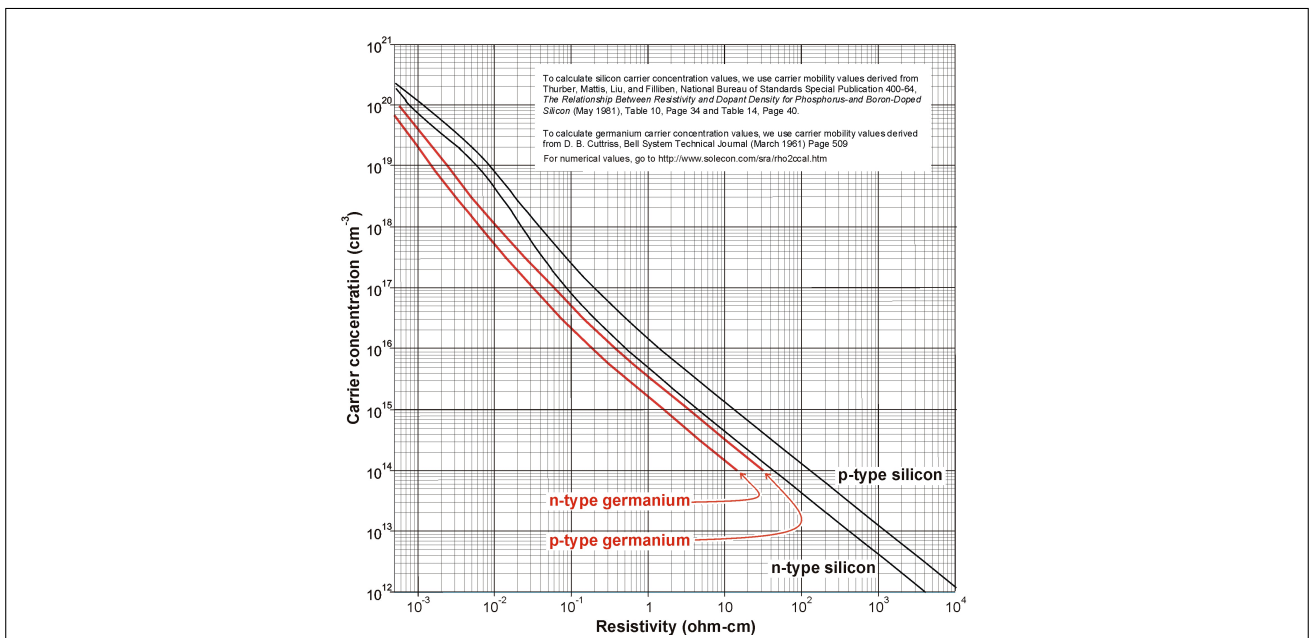


Figure 1: R-L-dopant relation

You can either use the graphics from Figure 1 and determine the dopant concentration graphically, which is very very imprecise or use a online tool like the one from Solecon¹

Germanium is being included in this graphics just in case someone is going to fork this process based on Germanium substrate.

¹<http://www.solecon.com/sra/rho2ccal.htm>

2 Infusion

The redistribution process depends on the ratio of the solubility of the doping material in silicon and SiO_2 . At the Si/ SiO_2 interface the dopants are redistributed by segregation until the ratio of their concentration at the interface is the same as the ratio of their solubility in both materials. The ratio of dopant solubility is expressed by the segregation coefficient m which is

$$m = \frac{\text{solubility in silicon}}{\text{solubility in SiO}_2} \quad (1)$$

As listed in Table 1 below there are dopant species which solubilize better in SiO_2 than in silicon ($m < 1$) and species which have a reversed behavior ($m > 1$). In case of $m < 1$, as for Boron, the dopant concentration is enhanced at the SiO_2 side, whereas beneath the interface, there is a dopant depletion at the silicon surface. For reversed solubility ratios ($m > 1$, like Phosphorus), only few dopant atoms penetrate the interface. In order to obtain the by m determined concentration ratio at the interface, dopant atoms from deeper silicon zones diffuse back to the surface zone. Therefore, the dopant concentration at the silicon surface is enhanced, as illustrated in Figure 2b. In Figure 2, C_c denotes the dopant concentration in the silicon surface zone before oxidation. x is the distance from the silicon surface.

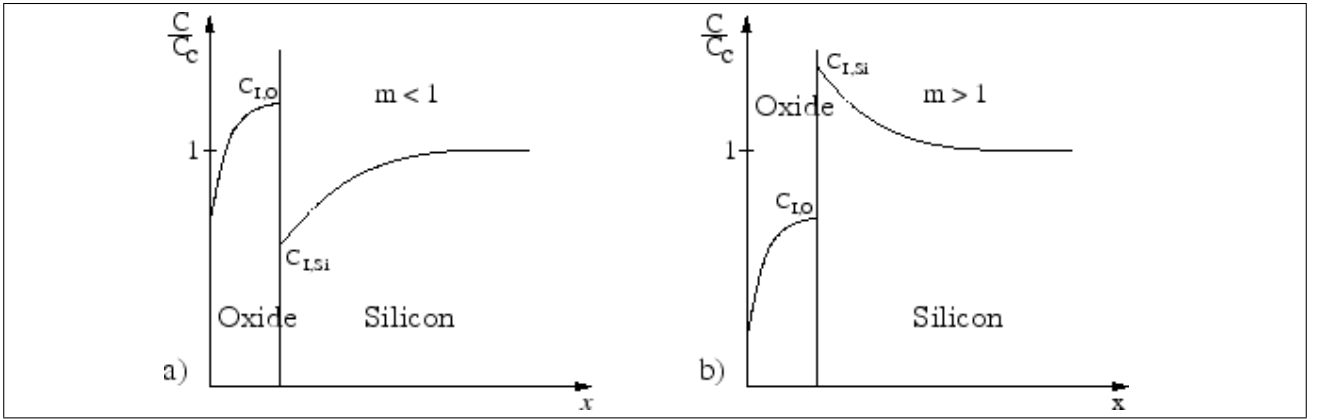


Figure 2: Schematic illustration of dopant redistribution

Dopant species	Boron	Phosphor	Antimon	Arsen	Gallium
m	0.1-0.3	10	10	10	20

Table 1: Segregation coefficients m for important dopant species in silicon

3 Constant source diffusion (Predeposition)

Although the diffusion process of donors and acceptors into the silicon crystal is a three dimensional process for simplicity we first only discuss the one dimensional mathematics for it in order to get a "simple" equation for the depth-time-temperature relation.

This is only valid for a constant source of dopants on the surface of the wafer (gas, for instance). These equations are used for predicting the pre-deposition step (in case this process would be adapted by someone for predeposition instead of ion implant)

We start with Ficks² law (for all German speakers: Yes that's his name) where the dopant concentration N is coupled with time and place

$$\frac{\partial N}{\partial t} = D \cdot \frac{\partial^2 N}{\partial x^2} \quad (2)$$

The diffusion coefficient is as well material as well as temperature dependent and can be calculated with the following equation:

$$D = D_0 \cdot \exp\left(-\frac{E_a}{k \cdot T}\right) \quad (3)$$

With $k = 8.62 \cdot 10^{-5} \frac{eV}{K}$ being the Boltzman constant and in table 3 we can see the D_0 and E_a values for the most common materials³ which we can use within the further calculations for our well dimensioning phases. The temperature usually is in the area of $1000^\circ C$ or $1273.15K$.

Element	D_0	$\left[\frac{cm^2}{s}\right]$	E_a [eV]
P	10.50		3.69
As	0.32		3.56
Sb	5.60		3.95
B	10.50		3.69
Al	8.00		3.47
Ga	3.60		3.51
Cu	0.0025		0.65

Table 2: D_0 and E_a values for boron and phosphorus

The law stated above

$$\frac{\partial N}{\partial t} = D \cdot \frac{\partial^2 N}{\partial x^2} \quad (4)$$

has the same form as the temperature conductivity equation (Laplace) for which we already have a general solution

$$\frac{\partial u}{\partial t} = a^2 \cdot \frac{\partial^2 u}{\partial x^2} \quad (5)$$

Which means that we can map the general solution for the temperature conductivity equations after Laplace

$$u(x, t) = \frac{1}{2 \cdot a \cdot \sqrt{\pi \cdot t}} \cdot \int_{-\infty}^{\infty} f(a) \cdot \exp\left(\frac{-(x-a)^2}{4 \cdot a^2 \cdot t^2}\right) da \quad (6)$$

to our Ficks law with $a = \sqrt{D}$ and $u = N$

$$N(x, t) = \frac{1}{2 \cdot \sqrt{D} \cdot \sqrt{\pi \cdot t}} \cdot \int_{-\infty}^{\infty} f(\sqrt{D}) \cdot \exp\left(\frac{-(x-\sqrt{D})^2}{4 \cdot D \cdot t^2}\right) da \quad (7)$$

with the edge conditions

$$N(x = 0, t > 0) = N_0 \quad (8)$$

$$N(x \geq 0, t = 0) = 0 \quad (9)$$

we get the resulting function from the solving process for the Laplace temperature conduction equations

$$u(x, t) = u_0 \cdot \operatorname{erfc}\left(\frac{x}{2 \cdot a \cdot \sqrt{t}}\right) \quad (10)$$

²https://en.wikipedia.org/wiki/Fick%27s_laws_of_diffusion

³ISBN 3-8023-1588:Hoppe Bernhard, Mikroelektronik 2, Page 24, Table 2.1

with the error function being an integral of the form

$$\operatorname{erfc}(z) = \left(1 - \frac{2}{\sqrt{\pi}}\right) \cdot \int_0^z e^{-a^2} da \quad (11)$$

Or in case of our dopant concentration equation we can replace a with the square root of the diffusion coefficient in order to get the error function for our dopant density equation:

$$\operatorname{erfc}(z) = \left(1 - \frac{2}{\sqrt{\pi}}\right) \cdot \int_0^z e^{-D} d\sqrt{D} \quad (12)$$

$$N(x, t) = N_0 \cdot \operatorname{erfc}\left(\frac{x}{2 \cdot \sqrt{D \cdot t}}\right) = N_0 \cdot \operatorname{erfc}\left(\frac{x}{x_l(t)}\right) \quad (13)$$

Now we can extract the layer thickness and the depth of the well in dependency of the time and the temperature, respectively:

$$x_l(t) = 2 \cdot \sqrt{D \cdot t} \quad (14)$$

$$x_l(t) = 2 \cdot \sqrt{D_0 \cdot \exp\left(-\frac{E_a}{k \cdot T}\right) \cdot t} \quad (15)$$

And plot the result for multiple different drive in times

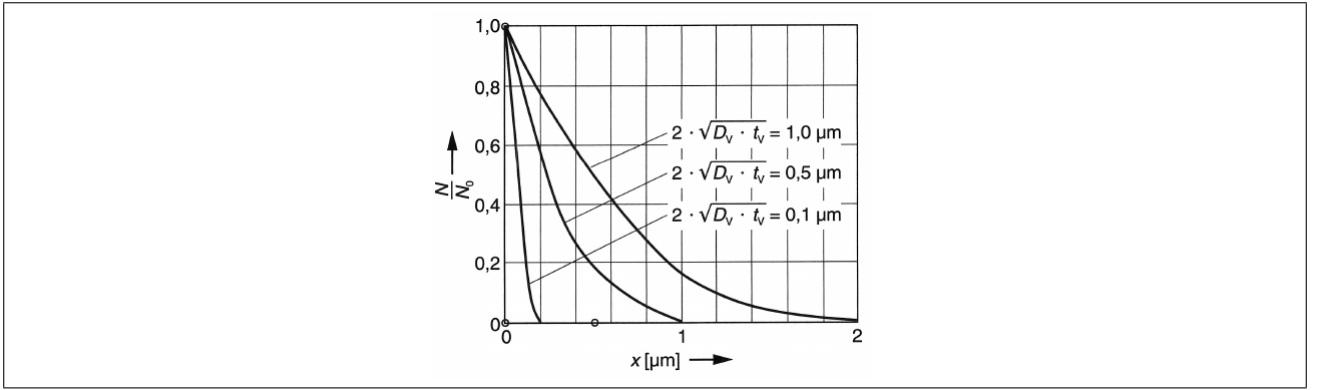


Figure 3: Different predeposition times

We can now describe the dosage based on the time and temperature of the diffusion

$$Q = \frac{2}{\sqrt{\pi}} \cdot N_0 \cdot \sqrt{D \cdot t} \quad (16)$$

Where N_0 (concentration at the surface) equals the maximum solubility of a given element (e.g. boron) within the given medium (e.g. silicon).⁴

⁴If someone really wants to do this in his basement he can google these values and make a pull request

4 Ion implant

We can use the following equation to calculate the carrier distribution after implantation:

$$N(x) = N_p \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right) = \frac{Q}{\sqrt{2\pi}\Delta R_p} \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right) \quad (17)$$

Where the projected range (R_p) and the projected straggle (ΔR_p) need to be looked up in tables ⁵ or looked up using an online tool like the one linked in the footnote ⁶

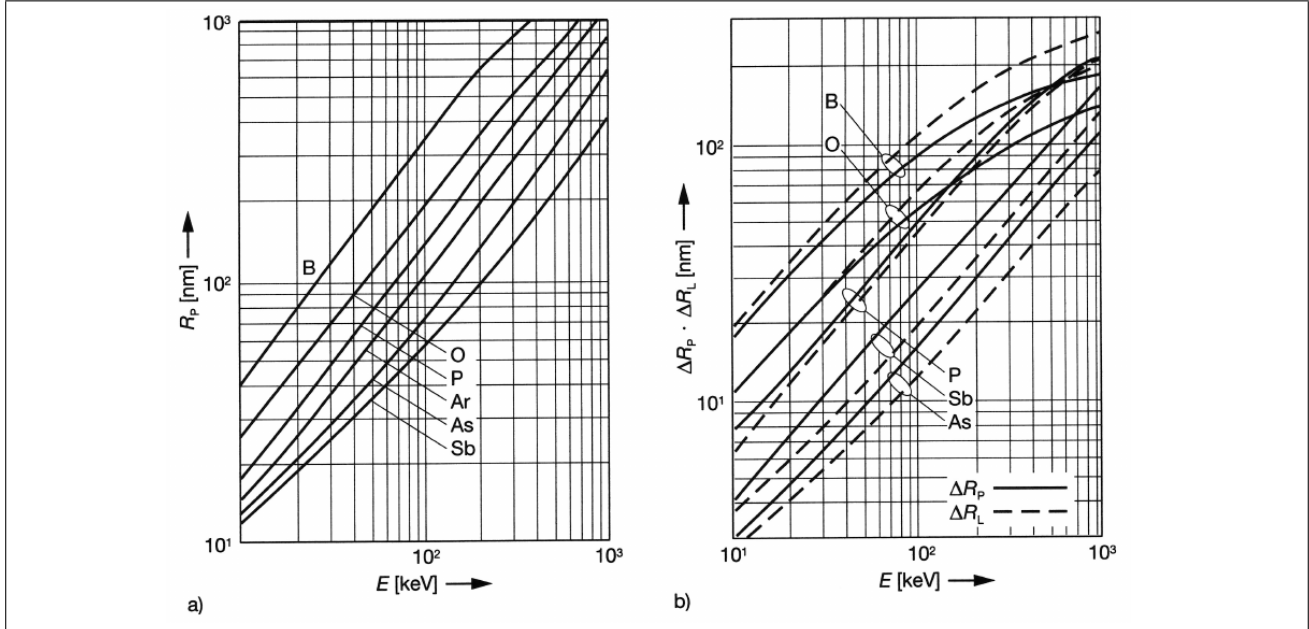


Figure 4: R_p and ΔR_p in silicon

If you do implant before the diffusion just set $x_v = R_p$

5 Drive-in (limited source diffusion)

After pre-deposition or ion implant of the initial dosage we need to drive in the ions deeper into the crystal. In order to prevent back-diffusion into the gas we seal off the oxide window with another layer of oxide in order to make sure that all the dopants stay inside the silicon crystal.

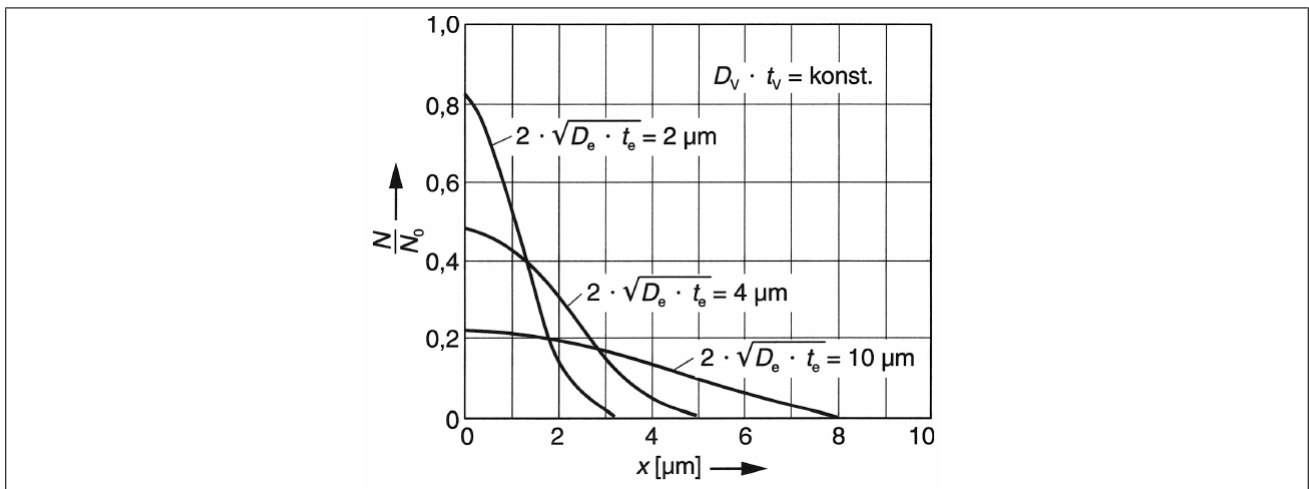


Figure 5: Drive-in well depths and concentrations

⁵ISBN 3-8023-1588:Hoppe Bernhard, Mikroelektronik 2, Page 48, Table 3.2

⁶<http://cleanroom.byu.edu/rangestruggle>

We set the condition that the pre-deposition/implant depth is much lower than the depth of the final diffused volume with the following inequation:

$$x_e = 2 \cdot \sqrt{D_e \cdot t_e} \gg 2 \cdot \sqrt{D_v \cdot t_v} = x_v \quad (18)$$

Where x_v is the the depth of the predeposition/implant step.

By neglecting the distribution thickness of the original implantation dosage and assuming that it's comparably thin compared to the medium thickness we can replace $f(a) \approx \delta(a)$ within Equation 7 which makes

$$N(x, t) = \frac{1}{2 \cdot \sqrt{D} \cdot \sqrt{\pi \cdot t}} \cdot \int_{-\infty}^{\infty} f(\sqrt{D}) \cdot \exp\left(\frac{-(x - \sqrt{D})^2}{4 \cdot D \cdot t}\right) da \quad (19)$$

become

$$N(x, t) = \frac{1}{2 \cdot \sqrt{D} \cdot \sqrt{\pi \cdot t}} \cdot \int_{-\infty}^{\infty} \delta(\sqrt{D}) \cdot \exp\left(\frac{-(x - \sqrt{D})^2}{4 \cdot D \cdot t}\right) da \quad (20)$$

and finally

$$N(x, t) = \frac{Q}{\sqrt{\pi \cdot D_e \cdot t}} \cdot \exp\left(\frac{-x^2}{4 \cdot D_e \cdot t}\right) \quad (21)$$

6 Vertical diffusion and junction formation (Well formation)

The goal of most diffusions is to form pn junctions by converting p-type material to n-type material or vice versa. In Figure 6, for example, the wafer is uniformly doped n-type material with a concentration indicated by N_B , and the diffusing impurity is boron. The point at which the diffused impurity profile intersects the background concentration is the metallurgical junction depth (x_j). The net impurity concentration at x_j is zero. Setting $N(x)$ equal to the background concentration N_B at $x = x_j$ yields⁷ for a fixed source

$$x_j = 2 \cdot \sqrt{D \cdot t \cdot \ln\left(\frac{N_0}{N_B}\right)} \quad (22)$$

and for a continuous source

$$x_j = 2 \cdot \sqrt{D \cdot t} \cdot \operatorname{erfc}^{-1}\left(\frac{N_B}{N_0}\right) \quad (23)$$

for the Gaussian and complementary error function distributions, respectively.

In Figure 6, the boron concentration N exceeds N_B to the left of the junction, and this region is p-type. To the right of x_j , N is less than N_B , and this region remains n-type.

To calculate the junction depth, we must know the background concentration N_B of the original wafer. Look at Figure 1 for this purpose.

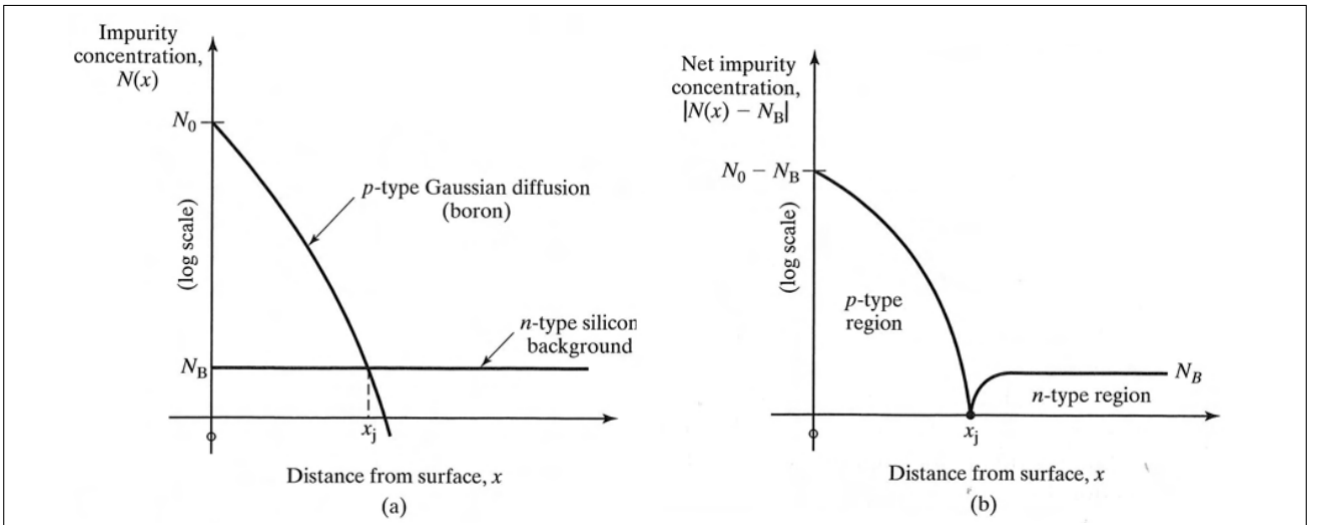


Figure 6: Formation of a pn junction by diffusion: (a) An example of a p-type Gaussian diffusion into a uniformly doped n-type wafer; (b) net impurity concentration in the wafer.

⁷Gerald W. Neudeck and Robert F. Pierret, Modular series on solid state devices, Volume V, Chapter 4

7 MOS Capacitance

https://ecee.colorado.edu/~bart/book/book/chapter6/ch6_3.htm

8 Threshold voltages (V_T)

The threshold voltage dependence on the doping density is illustrated with Figure 7 for both n-type and p-type MOSFETs with an aluminum gate metal.

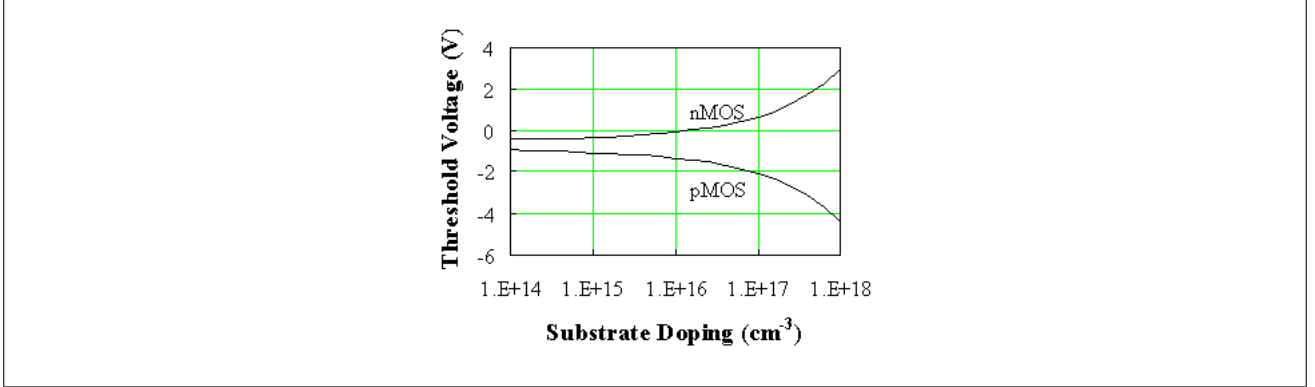


Figure 7: Threshold voltage of n-type (upper curve) and p-type (lower curve) MOSFETs versus substrate doping density.

We can directly switch $\frac{J}{C}$ with Volts because these two units are equal!^a Also V_{th} will be treated as a constant for any further calculations within this document.

The same goes for the eV to V conversion, wherever we have work functions to potentials because (e.g. Φ_M for Aluminum): $4.1eV \approx 6.5689241452810^{-19}J$

$$\Phi_M = \frac{E_M}{q} = \frac{4.1eV}{q} = \frac{6.5689241452810^{-19}J}{q} = \frac{6.5689241452810^{-19}J}{1.60217663410^{-19}C} \approx 4.099999966220953 \frac{J}{C} = \underline{4.1V}$$

^a<https://en.wikipedia.org/wiki/Volt>

The formula for calculating the threshold voltage of a MOS device is the following:

$$V_T = V_{t-mos} + V_{FB} \quad (24)$$

where V_{t-mos} is the threshold voltage of an ideal MOS capacitor, V_{FB} is the flat-band voltage and V_{t-mos} is the threshold. The MOS threshold voltage, V_{t-mos} is calculated by considering the MOS capacitor structure that form the gate of the MOS transistor.

The ideal threshold voltage may be expressed as:

$$V_{t-mos} = 2\phi_F + \frac{Q_b}{C_{ox}} \quad (25)$$

$$Q_b = \sqrt{2\epsilon_{Si} \cdot q \cdot N \cdot (|2\phi_F| + V_{SB})} \quad (26)$$

where C_{ox} is the oxide capacitance and Q_b which is called the bulk charge term.

The bulk potential is given for P substrate (V_{Tp})

$$\phi_{Fp} = V_{th} \cdot \ln \left(\frac{N_p}{N_i} \right) \quad (27)$$

and N substrate (V_{Tn}), respectively:

$$\phi_{Fn} = V_{th} \cdot \ln \left(\frac{N_i}{N_n} \right) \quad (28)$$

V_{th} is the thermal voltage.⁸

$$V_{th} = \frac{kT}{q} \approx 0.026 \frac{J}{C} = 0.026V = 26mV \quad (29)$$

Since we connect bulk and source $V_{SB} = 0$ we can simplify the equation to become

$$Q_b = \sqrt{2 \cdot \epsilon_{Si} \cdot q \cdot N \cdot (|2 \cdot \phi_F|)} \quad (30)$$

⁸https://en.wikipedia.org/wiki/Boltzmann_constant#Role_in_semiconductor_physics:_the_thermal_voltage

$$Q_b = 2 \cdot \sqrt{\epsilon_{Si} \cdot q \cdot N \cdot |\phi_F|} \quad (31)$$

V_{FB} , is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho(x) dx \quad (32)$$

Because we're not yet dealing with non-volatile memory devices which contain an oxide surface state charge we can just $\rho(x) = 0$. Q_{SS} is a value which has to be measured.

$$V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{ox}} \quad (33)$$

This brings us to a general equation for the threshold voltage V_T :

$$V_T = 2\phi_F + \frac{2 \cdot \sqrt{\epsilon_{Si} \cdot q \cdot N \cdot |\phi_F|}}{C_{ox}} + \phi_{MS} - \frac{Q_{SS}}{C_{ox}} \quad (34)$$

With the variables and constants being the following for both sub chapters:

- N_i is the carrier concentration in intrinsic (undoped) silicon. N_i is equal to $1.45 \times 10^{10} cm^{-3} = 1.45 \times 10^{16} m^{-3}$ at $300^\circ K$
- Q_{SS} depends on the process and is measured. Usually it's between $10^9 \frac{1}{cm^2}$ and $10^{10} \frac{1}{cm^2}$ ergo $Q_{SS} = q \cdot 10^{10} \frac{1}{cm^2} = 1.6 \cdot 10^{-5} \frac{C}{m^2}$
- $E_M = q \cdot \phi_M = 4.1 eV$ is the "work function" of our metal at the gate (Aluminum)
- $E_g = E_g(300)[eV]$
 $E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} = 1.166 - 4.73 \cdot 10^{-4} \cdot \frac{T^2}{T + 636} [eV]$ is the band gap energy of silicon at a given temperature⁹ for which the parameters can be taken from [Table 3](#)

	Germanium	Silicon	GaAs
$E_g(0)[eV]$	0.7437	1.166	1.519
$\alpha[eV/K]$	4.77×10^{-4}	4.73×10^{-4}	5.41×10^{-4}
$\beta[K]$	235	636	204

Table 3: Band cap energy parameters

- $C_{ox} [\frac{F}{m^2}]$ is the capacity of the gate oxide
- $\epsilon_0 = 8.85 \cdot 10^{-14} \frac{F}{cm} = 8.85 \cdot 10^{-12} \frac{F}{m}$ is the electric permittivity in vacuum
- $\epsilon_{Si} = 11.68 \cdot \epsilon_0$ is the relative permittivity of silicon
- $\epsilon_{ox} = 3.9 \cdot \epsilon_0$ is the relative permittivity of silicon oxide
- $t_{ox}[cm]$ is the thickness of the oxide layer in cm
- $E_{ef} = q \cdot \chi = 4.05 eV$ is the electron affinity of a silicon crystal surface¹⁰
- $q = 1.602 \cdot 10^{-19} C$ is the elementary charge
- $k = 1.38064852 \cdot 10^{-23} \frac{J}{K}$ is the Boltzmann constant
- $T = 300 K$ the temperature, which we assume to be the room temperature for simplicity further on in this document as well.

⁹<https://ecee.colorado.edu/~bart/book/eband5.htm>

¹⁰https://en.wikipedia.org/wiki/Electron_affinity

8.1 Threshold voltage with metal gate (V_T)

V_{FB} is the flat band voltage and is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{ox}} = \phi_M - \phi_S - \frac{Q_{SS}}{C_{ox}} \quad (35)$$

With

$$\phi_S = \chi + \frac{E_g}{2q} + \phi_F \quad (36)$$

we get

$$V_{FB} = \phi_M - \left(\chi + \frac{E_g}{2q} + \phi_F \right) - \frac{Q_{SS}}{C_{ox}} \quad (37)$$

And because of the simplifications we did to F_{FB} we get to:

$$V_T = 2\phi_F + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_F| \cdot N}}{C_{ox}} + V_{FB} \quad (38)$$

$$V_T = 2\phi_F + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_F| \cdot N}}{C_{ox}} + \phi_M - \left(\chi + \frac{E_g}{2q} + \phi_F \right) - \frac{Q_{SS}}{C_{ox}} \quad (39)$$

$$V_T = 2\phi_F + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_F| \cdot N}}{C_{ox}} + \phi_M - \chi - \frac{E_g}{2q} - \phi_F - \frac{Q_{SS}}{C_{ox}} \quad (40)$$

$$V_T = \phi_F + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_F| \cdot N}}{C_{ox}} + \phi_M - \chi - \frac{E_g}{2q} - \frac{Q_{SS}}{C_{ox}} \quad (41)$$

The contact potential from the Aluminum contact to the surface of the gate (silicon below the oxide) is fixed for $T = 300^\circ K$:

$$\phi_M - \chi - \frac{E_g}{2q} = 4.1V - 4.05V - \frac{1.12eV}{2q} = 4.1V - 4.05V - 0.56V = -0.51V \quad (42)$$

From that we get

$$V_T = \phi_F + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_F| \cdot N}}{C_{ox}} - 0.51V \quad (43)$$

Now we can calculate the thresholds for P substrate (V_{Tp}) and N substrate (V_{Tn}), respectively the wells we build on unpredoped substrated, which makes the equation for single-doped substrate valid for both wells with Which brings us to the equations for the N-channel and P-channel thresholds:
(N-Channel MOSFETs are built on p-substrate)

$$V_{Tn} = \phi_{Fp} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fp}| \cdot N}}{C_{ox}} - 0.51V \quad (44)$$

(P-Channel MOSFETs are built on n-substrate)

$$V_{Tp} = \phi_{Fn} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fn}| \cdot N}}{C_{ox}} - 0.51V \quad (45)$$

This equation will be used further on to find the optimum gate oxide thickness for our transistors.

8.2 Threshold voltage with poly silicon gate (V_T)

V_{FB} is the flat band voltage and is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{ox}} \quad (46)$$

The term ϕ_{MS} is the work function difference between the gate material and the silicon substrate ($\phi_{gate} - \phi_{Si}$), which may be calculated for an n+ gate over a p substrate

$$\phi_{MSp} = -\left(\frac{E_g}{2} + \phi_{Fp}\right) \quad (47)$$

and for an n+ poly gate on an n-substrate

$$\phi_{MSn} = -\left(\frac{E_g}{2} - \phi_{Fn}\right) \quad (48)$$

Now we can calculate the thresholds for P substrate (V_{Tp}) and N substrate (V_{Tn}), respectively the wells we build on unpredoped substrated, which makes the equation for single-doped substrate valid for both wells. (N-Channel MOSFETs are built on p-substrate)

$$V_{Tn} = 2 \cdot \phi_{Fp} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fp}| \cdot N_p}}{C_{ox}} + \phi_{MSp} - \frac{Q_{SS}}{C_{ox}} \quad (49)$$

$$V_{Tn} = 2 \cdot \phi_{Fp} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fp}| \cdot N_p}}{C_{ox}} - \frac{E_g}{2} - \phi_{Fp} - \frac{Q_{SS}}{C_{ox}} \quad (50)$$

$$V_{Tn} = \phi_{Fp} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fp}| \cdot N_p}}{C_{ox}} - \frac{E_g}{2} - \frac{Q_{SS}}{C_{ox}} \quad (51)$$

(P-Channel MOSFETs are built on n-substrate)

$$V_{Tp} = 2 \cdot \phi_{Fn} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fn}| \cdot N_n}}{C_{ox}} + \phi_{MSn} - \frac{Q_{SS}}{C_{ox}} \quad (52)$$

$$V_{Tp} = 2 \cdot \phi_{Fn} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fn}| \cdot N_n}}{C_{ox}} - \frac{E_g}{2} + \phi_{Fn} - \frac{Q_{SS}}{C_{ox}} \quad (53)$$

$$V_{Tp} = 3 \cdot \phi_{Fn} + \frac{2\sqrt{\epsilon_{Si} \cdot q \cdot |\phi_{Fn}| \cdot N_n}}{C_{ox}} - \frac{E_g}{2} - \frac{Q_{SS}}{C_{ox}} \quad (54)$$

This equation will be used further on to find the optimum gate oxide thickness for our transistors.

9 Threshold voltage (V_T) adjustment

At some point in the future this will be of very high relevance, because the lower the size of the transistors becomes, the higher the offset to V_{Tp} and V_{Tn} needs to be in order to stay on TTL 5V logic level, or at least compensate for the lowered voltages in order to reach the 3.3V CMOS logic levels.

Adjustment of the threshold voltage can be achieved by:

- A relatively small dose N_I (units: ions/cm²) of dopant atoms is implanted into the near-surface region of the semiconductor.
- When the MOS device is biased in depletion or inversion, the implanted dopants add to (or subtract from) the depletion charge near the oxide-semiconductor interface

The formula to calculate the voltage offset is:

$$\Delta V_T = -\frac{qN_I}{C_{ox}} \begin{cases} N_I > 0 \text{ for donor atoms (Phosphorus/N)} \\ N_I < 0 \text{ for acceptor atoms (Boron/P)} \end{cases} \quad (55)$$