

Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells¹ and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

¹<https://github.com/chipforge/StdCellLib>

Libre Silicon process design rules

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1 Layer Definitions

Name	GDSII	CIF	Description
PWELL	41	CWP	p-well
NWELL	42	CWN	n-well
ACTIVE	43	CAA	active area
PPLUS	44	CSP	p^+ implant
NPLUS	45	CSN	n^+ implant
POLY	46	CPG	poly silicium
CONTACT	25	CCC	contact (connects METAL1 to POLY)
METAL1	49	CM1	lowest metal layer
VIA1	50	CV1	via layer (connects METAL2 to METAL1)
METAL2	51	CM2	second metal layer
VIA2	61	CV2	via layer (connects METAL3 to METAL2)
METAL3	62	CM3	third metal layer
GLASS	52	COG	passivation / isolation

2 General Requirements

- 1.1 All scaled dimensions are specified in Lambda λ .
- 1.2 All fixed dimensions are specified in Microns μm .
- 1.3 All geometries must be drawn on grid. The grid size is 1λ .
- 1.4 Polygons should be rectangles with 90 degree angles only.
- 1.5 The die size should be an integer multiple of $10\mu m$.

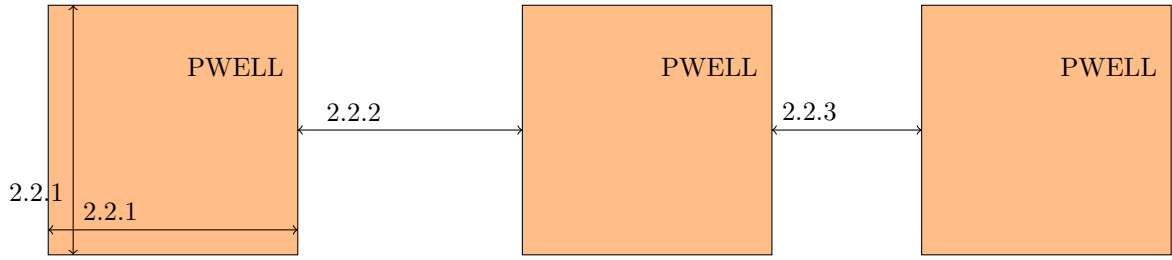
Node	λ	2λ
1 micron	500nm	$1\mu m$
0.5 micron	250nm	500nm
0.25 micron	125nm	250nm

3 Process Layer Overview

Name	Minimum Width	Minimum Spacing
PWELL	10λ	10λ
NWELL	10λ	10λ
ACTIVE	3λ	3λ
POLY	2λ	2λ
CONTACT	2λ	2λ
METAL1	4λ	4λ
VIA1	2λ	3λ
METAL2	4λ	4λ
VIA2	2λ	3λ
METAL3	6λ	4λ

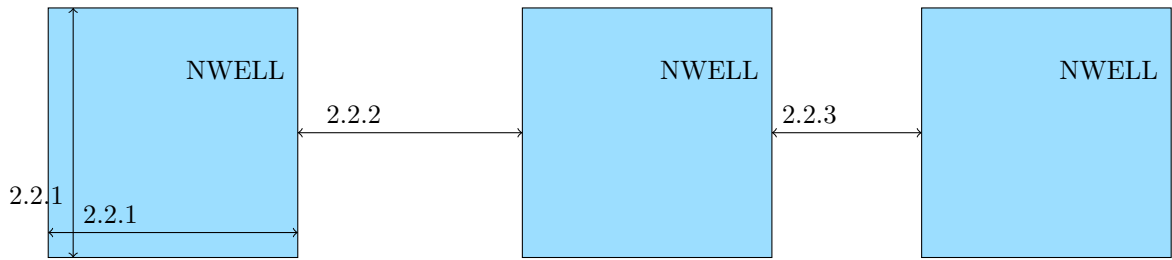
4 Structure Rules

4.1 PWELL Rules



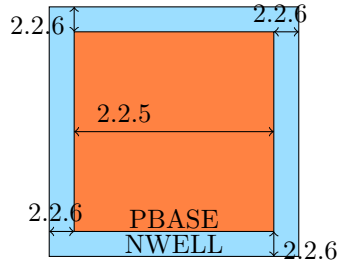
- 2.1.1 Minimum Width of PWELL is 10λ .
- 2.1.2 Minimum Spacing to PWELL at different potential is 10λ .
- 2.1.3 Minimum Spacing to PWELL at same potential is 0λ .
- 2.1.4 Minimum Spacing to NWELL is 12λ .

4.2 NWELL Rules



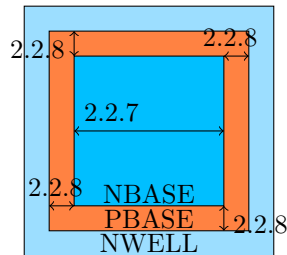
- 2.2.1 Minimum Width of NWELL is 10λ .
- 2.2.2 Minimum Spacing to NWELL at different potential is 10λ .
- 2.2.3 Minimum Spacing to NWELL at same potential is 0λ .
- 2.2.4 Minimum Spacing to PWELL is 12λ .

4.3 PBASE Rules



- 2.2.5 Minimum Width of PBASE is 10λ .
- 2.2.6 Minimum Overlap of PBASE to NWELL is 5λ .

4.4 NBASE Rules

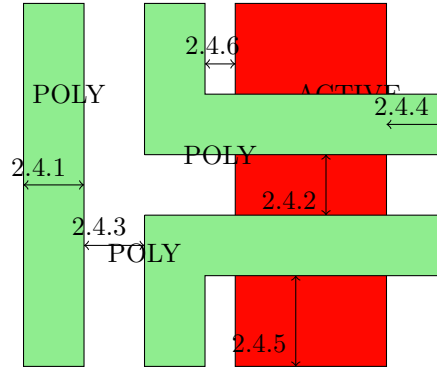


- 2.2.7 Minimum Width of NBASE is 10λ .
- 2.2.8 Minimum Overlap of NBASE to PBASE is 5λ .

4.5 ACTIVE Rules

2.3.1	Minimum Width of ACTIVE is	3 λ .
2.3.2	Minimum Spacing to ACTIVE is	3 λ .
2.3.3	Minimum Source/Drain surround by PWELL/NWELL is	6 λ .
2.3.4	Minimum Substrate/NWELL contact sourround by PWELL/NWELL is	3 λ .
2.3.5	Minimum Spacing to ACTIVE of opposite type is	4 λ .

4.6 POLY Rules



2.4.1	Minimum Width of POLY is	2 λ .
2.4.2	Minimum Spacing to POLY over ACTIVE is	2 λ .
2.4.3	Minimum Spacing to POLY over others is	2 λ .
2.4.4	Minimum Gate extension beyond ACTIVE is	2 λ .
2.4.5	Minimum ACTIVE extension beyond POLY is	3 λ .
2.4.6	Minimum Spacing of POLY to ACTIVE is	1 λ .

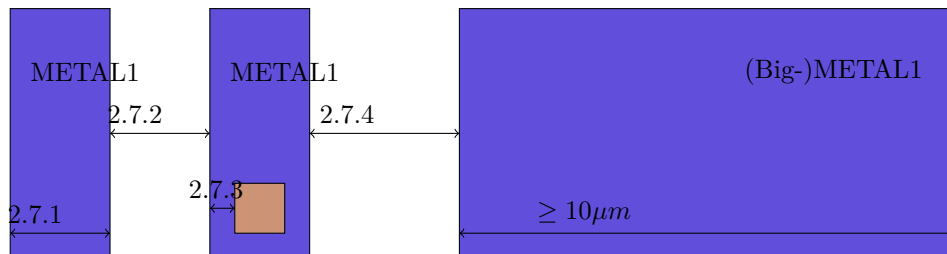
4.7 NPLUS/PPLUS Rules

2.5.1	Minimum Spacing to POLY is	3 λ .
2.5.2	Minimum Overlap to ACTIVE is	2 λ .
2.5.3	Minimum Overlap to CONTACT is	1 λ .

4.8 CONTACT Rules

2.6.1	Exact Width/Height of CONTACT is	2 $\lambda \times 2\lambda$.
2.6.2	Minimum Overlap by POLY or ACTIVE is	1 λ .
2.6.3	Minimum Spacing to CONTACT is	2 λ .
2.6.4	Minimum Spacing to Gate is	2 λ .
2.6.5	Minimum Spacing of POLY CONTACT to other POLY is	4 λ .
2.6.6	Minimum Spacing of ACTIVE CONTACT to POLY CONTACT is	4 λ .

4.9 METAL1 Rules

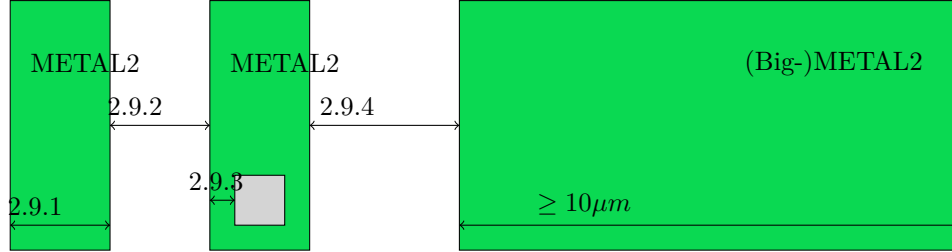


2.7.1	Minimum Width of METAL1 is	4 λ .
2.7.2	Minimum Spacing of METAL1 is	4 λ .
2.7.3	Minimum Overlap of CONTACT or VIA is	1 λ .
2.7.4	Minimum Spacing to METAL1 for lines wider than 10 μm is	6 λ .

4.10 VIA1 Rules

2.8.1	Exact Width/Height of VIA1 is	$2\lambda \times 2\lambda$.
2.8.2	Minimum Spacing to VIA1 is	3λ .
2.8.3	Minimum Spacing to CONTACT is	2λ .
2.8.4	Minimum Spacing to POLY or ACTIVE is	2λ .

4.11 METAL2 Rules

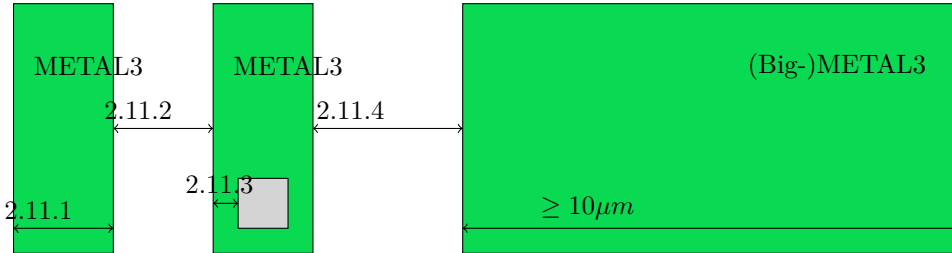


2.9.1	Minimum Width of METAL2 is	4λ .
2.9.2	Minimum Spacing to METAL2 is	4λ .
2.9.3	Minimum Overlap to VIA1 is	1λ .
2.9.4	Minimum Spacing to METAL2 for lines wider than $10\mu m$ is	6λ .

4.12 VIA2 Rules

2.10.1	Exact Width/Height of VIA2 is	$2\lambda \times 2\lambda$.
2.10.2	Minimum Spacing to VIA2 is	3λ .

4.13 METAL3 Rules



4.11.1	Minimum Width of METAL3 is	6λ .
2.11.2	Minimum Spacing to METAL3 is	4λ .
2.11.3	Minimum Overlap to VIA2 is	1λ .
2.11.4	Minimum Spacing to METAL3 for lines wider than $10\mu m$ is	6λ .

4.14 GLASS Rules

2.12.1	Exact Width/Height of GLASS is	$120\lambda \times 120\lambda$.
2.12.2	Minimum METAL3 Overlap of GLASS opening is	12λ .
2.12.3	Minimum Spacing of pad METAL3 to unrelated METAL is	$30\mu m$.
2.12.4	Minimum Spacing of pad METAL3 to ACTIVE or POLY is	$15\mu m$.