

# Pad Library design concept for Libresilicon node LS1U

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## **Abstract**

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells and related free technology nodes from the LibreSilicon project.

# Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>Library contents and derivation of cells</b>	<b>3</b>
2.1	<b>CORNER</b> Corner cell for padding formation . . . . .	3
2.2	<b>PADANA</b> Pass-through pad for analog applications . . . . .	4
2.3	<b>PADFILL</b> Dummy (filler) pad . . . . .	4
2.4	<b>PADGND</b> Ground (negative supply) connection . . . . .	5
2.5	<b>PADVDD</b> Positive supply connection . . . . .	5
2.6	<b>PADGIO</b> General-purpose bidirectional digital pad . . . . .	6
2.7	<b>PADCIN</b> CMOS-level compatible input . . . . .	7
2.8	<b>PADTIN</b> TTL-level compatible input . . . . .	7
2.9	<b>PADCOUT</b> Digital output . . . . .	8
2.10	<b>PADTOUT</b> Digital output . . . . .	8
2.11	<b>PADOC</b> Open-drain current-driving output . . . . .	8
<b>3</b>	<b>ESD protection concept</b>	<b>9</b>
<b>4</b>	<b>Validation and characterization plan</b>	<b>10</b>
<b>5</b>	<b>Characterization, functional validation</b>	<b>10</b>
<b>6</b>	<b>Injection coupling test</b>	<b>10</b>
<b>7</b>	<b>ESD characterization</b>	<b>11</b>
<b>8</b>	<b>Further improvements</b>	<b>11</b>
<b>9</b>	<b>References</b>	<b>11</b>

# 1 Introduction

This document is intended to provide an overview of the design concept of the pad cell library for Libresilicon project's LS1U CMOS technology node. This document is a living document: it is expected to change throughout the development process.

## 2 Library contents and derivation of cells

The assortment of cells within the library is selected to satisfy most of the needs encountered in solitary digital based and mixed-signal applications, while keeping the complexity of the design effort reasonably low. The library is intended to be used for automatic generation of the padding of the chip by a higher-level synthesis or Place-and-Route tool, without needing to deal with detailed electrical design and layout considerations at system level. Since pads for applications like high-voltage or RF signals require application-specific and varying design without the possibility to provide off-the-self solutions, these are excluded from the scope of the library. The following cells are included:

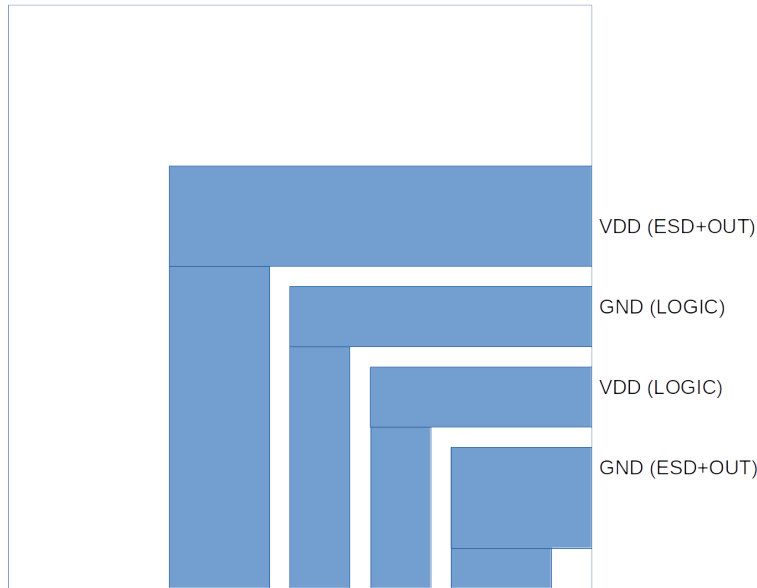
- **CORNER**
- **PADANA**
- **PADFILL**
- **PADGND**
- **PADVDD**
- **PADGIO**
- **PADCIN**
- **PADTIN**
- **PADCOUT**
- **PADTOUT**
- **PADOC**

The design effort should be started with designing **PADGIO**, then **CORNER**, followed by manual derivation of **PADVDD** and **PADGND**, and a tapeout and exhaustive test of the testchip. This may require multiple iterations to have the performance and robustness against ESD optimized. Then, manual derivation of **PADCIN**, **PADTIN**, **PADCOUT**, **PADTOUT**, **PADOC**, **PADANA** and **PADFILL** may follow. Due to the one-off nature of the design (it shall not be modified by the user unless extensive validation is performed on its behalf), the approach of creating and distributing an algorithm only, that generates the cells automatically, is not recommended.

The description of these pad cells are provided in the following sections.

### 2.1 CORNER Corner cell for padding formation

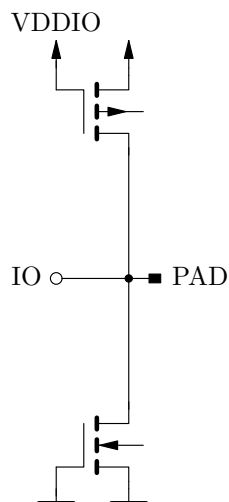
This cell does not contain active circuitry. It is intended to form a continuous padding by connecting the ends of the perpendicular rows of cells at the outer corners of the chip.

Simplified layout of **CORNER** cell

At least four global power supply lines should be supported, **VDDIO** and **VSSIO** as well as **VDDC** and **VSSC**. This means, there are two 'dirty' power supply lines dedicted for the io pad frame (big metal), and two 'core' power supply lines nicely filtered and according to the internal voltage level for the core logic. Both domains, for the io pad supply and the core supply should be de-coupled.

## 2.2 PADANA Pass-trough pad for analog applications

This cell is intended to provide transparent connection to the pad for analog signals, while providing ESD protection for the circuits behind it. It is derived from **PADGIO**, by removing input stage, output driver stage, and configuring both ESD transistors as GGNMOS/GGPMOS.

Schematic of **PADANA** cell

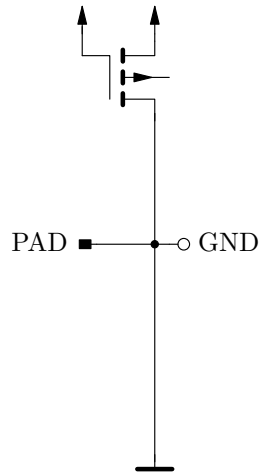
## 2.3 PADFILL Dummy (filler) pad

This cell does not contain active circuitry. It is intended as a placeholder to avoid interruption of the row of pad cells if no pad is desired at the given location, or if the pad is intended to be left unconnected. It is derived from **PADANA**, by means of removing ESD transistors.

## 2.4 **PADGND** Ground (negative supply) connection

This cell is intended to provide ground connection for the chip, including connection to the ground buses of the pading. It is derived from **PADANA** by removing the n-channel GGNMOS and shorting the pad connection to the ground bus via MET1-MET2 vias. Schematic of **PADANA** cell

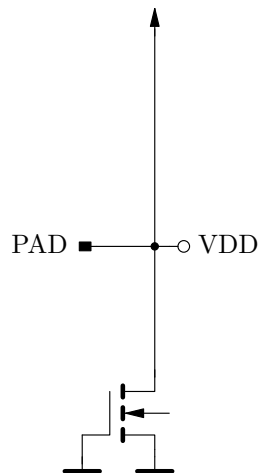
Schematic of **PADGND** cell



## 2.5 **PADVDD** Positive supply connection

This cell is intended to provide positive supply connection for the chip, including connection to the supply buses of the pading. It is derived from **PADANA** by removing the p-channel GGPMOS and shorting the pad connection to the supply bus via MET1-MET2 vias.

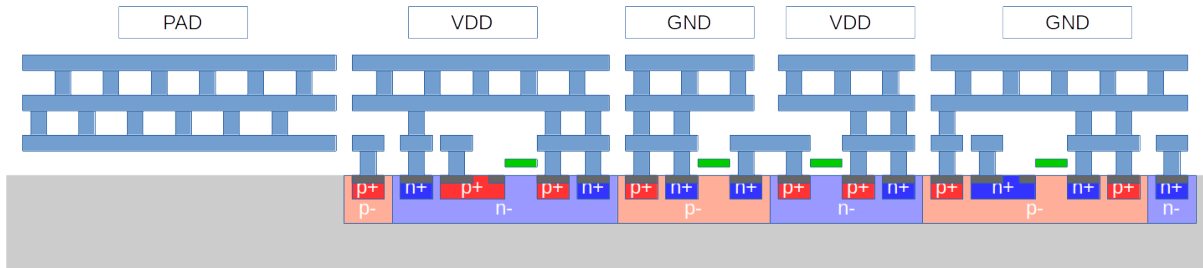
Schematic of **PADVDD** cell



Simplified cross-sectional layout of **PADVDD** and **PADGND** cells

## 2.6 PADGIO General-purpose bidirectional digital pad

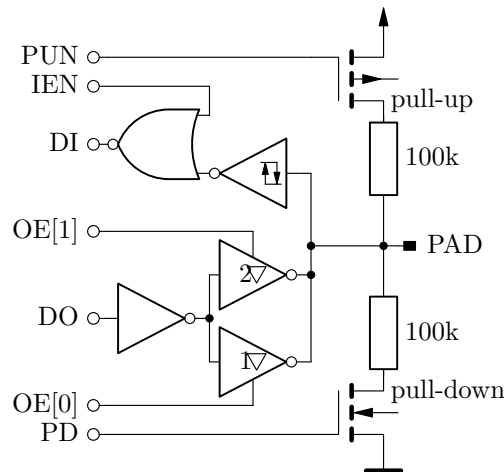
This cell is a general-purpose bidirectional digital pad, and also the design basis for most of the other cells. The cell can be subdivided into three parts: the actual bonding pad, the output stage transistors that also double as ESD supressor devices, and the input and control circuitry.

Simplified cross-sectional layout of **PADGIO** cell

The bonding pad is implemented as three metal plates on the three metal layers of LS1U. They are connected together by an array of vias in a chessboard-like structure. This ensures that the top metal layer is mechanically anchored to the underlying LTO layer, and will not delaminate during bonding and encapsulation.

The output stage transistors are surrounded by a double guardring to prevent latch-up if the pin is overloaded while the chip is biased. During characterization, this guardring may be removed. The outer guardrings also act as the substrate connection of the input and control circuitry transistors.

Schematic of **PADGIO** cell



**PADGIO** has additional features for more general usages as adaptable driver strength well as switchable pull-up and pull-down. The driver strength is regulated with the OE[1:0] port. Please have a look at the following table.

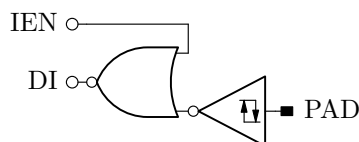
OE[1:0]	strength
0 0	-off-
0 1	1x
1 0	2x
1 1	3x

This feature allows applications to tune the driven strength dynamically.

## 2.7 PADCIN CMOS-level compatible input

This cell is a digital input with CMOS compatible input voltage levels. It is derived from **PADGIO** pad cell functionality.

### Schematic of **PADCIN** cell



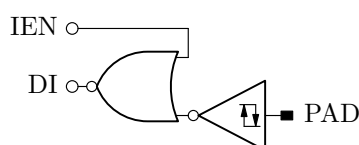
$V_{IL}$	$V_{IH}$
0 .. 1/3 VDD	2/3 VDD .. VDD

Input voltages above  $V_{IL}$  and below  $V_{IH}$  are ignored by the Schmitt-Trigger hysteresis.

## 2.8 PADTIN TTL-level compatible input

This cell is a digital input with TTL compatible input voltage levels. It is derived from **PADGIO** pad cell functionality.

Schematic of **PADCIN** cell



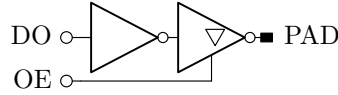
$V_{IL}$	$V_{IH}$
0 .. 0.8V	2V .. 5V

Input voltages above  $V_{IL}$  and below  $V_{IH}$  are ignored by the Schmitt-Trigger hysteresis. This cell is feasible with  $V_{DDIO} = 5$  Volt applications only.

## 2.9 PADCOUT Digital output

This cell is a digital output with CMOS-level compatible outputs. It is derived from **PADGIO** pad cell functionality.

Schematic of **PADTOUT** cell

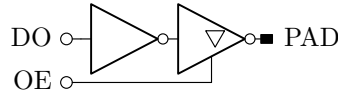


$V_{OL}$	$V_{OH}$
0 .. 1/5 VDD	4/5 VDD .. VDD

## 2.10 PADTOUT Digital output

This cell is a digital output with TTL-level compatible outputs. It is derived from **PADGIO** pad cell functionality.

Schematic of **PADTOUT** cell



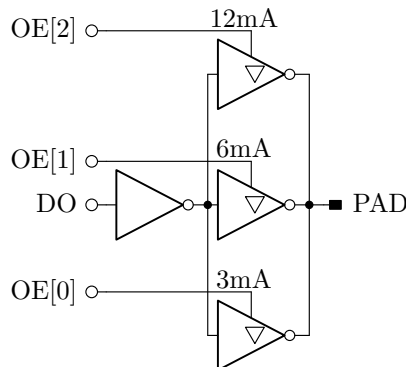
$V_{OL}$	$V_{OH}$
0 .. 0.4V	2.4V .. 5V

This cell is feasible with  $V_{DDIO} = 5$  Volt applications only.

## 2.11 PADOE Open-drain current-driving output

This cell is used for driving loads, eg. Light-emitting diodes (LED) without any additional external line resistor. Or, to drive CCITT current loops. Hence the internal current-mirror can be adjusted with  $OE[2:0]$  to different values regarding the following table.

Schematic of **PADOE** cell



This feature allows applications to tune the current dynamically instead of just switching as an open-collector output would do. Functionally it is comparable with a 3-bit Digital-Analog-Converter (DAC) in one pad cell.



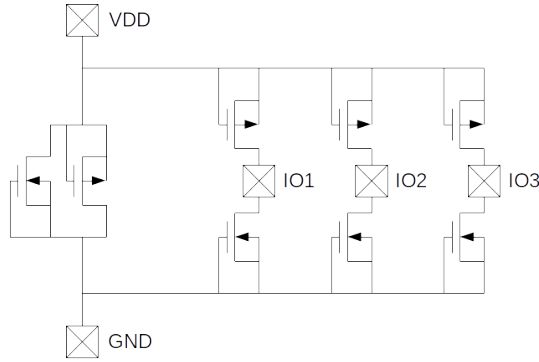
OE[2:0]			current [mA]
0	0	0	-
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	15
1	1	0	18
1	1	1	21

$V_{IL}$	$V_{IH}$
0 .. 1/5 VDD	4/5 VDD .. VDD

### 3 ESD protection concept

The basic principle of the ESD design is to provide a sufficiently low impedance path between any two of the pins of the IC. When used correctly, a padding formed from this library implements a chip-level ESD protection network similar to the one described in [1] 5.4.2.. Each electrically connected non-power pad has two ESD supressor devices: one GGNMOS to GND and one GGPMOS to VDD. These provide protection in case of pin-pin, pin-GND and pin-VDD discharges. The VDD and GND rings are designed to have sufficiently low impedance. To provide protection against VDD-GND discharges, a power clamp implemented as parallel-connected GGPMOS and GGNMOS devices is distributed along all **PADVDD** and **PADGND** cells. The current design goal for the ESD protection is to withstand a load equivalent to a 1KV HBM event. According to experience, this rating, although low, is sufficient to survive handling in both industrial mass-production and hobbyist environments with reasonable safety when sufficient ESD protection measures are in place. In later design iterations of the library, this rating may be increased as needed or possible.



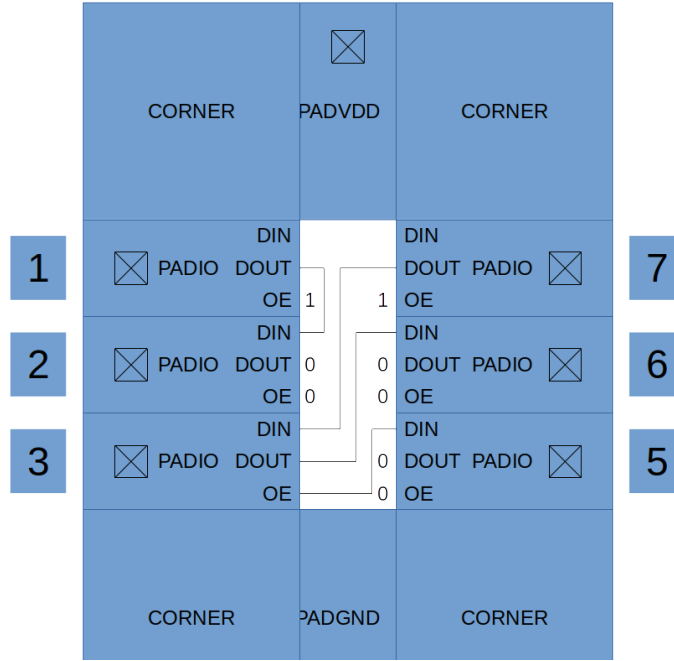
Chip-level ESD protection concept

The core part of pin-level ESD protection design is the low-side GGNMOS device that is also used as output transistor where needed. The high-side GGPMOS is derived from it by inverting the doping of the respective regions. The GGNMOS is implemented as a multi-finger structure, with individual fingers having an artificially increased resistance in the drain in order to ensure that the lowest voltage drop yielding to sufficiently high current to cause thermal failure is higher than the highest triggering voltage within the array. This increased impedance is then compensated by connecting multiple fingers in parallel, thus reducing the current through individual fingers, and consequentially, the overall voltage drop. In the initial design, the resistance is increased by lengthening the drain diffusion and introducing a portion that is masked by a nitride strip during silicide formation. In the possession of detailed fault analysis results after ESD zapping tests, the dimensioning of these geometries may be optimized in an iterative process. A feature of the GGNMOS structure is that it is formed

using the same layers and doping concentrations that are used to form the core logic, ensuring the correlation between the triggering voltage of the GGNMOS and the junction breakdown voltage of core logic transistors. It is assumed that the n+/pwell and p+/nwell breakdown voltages are lower than the gate oxide breakdown voltage (design target for oxide is 40V), therefore no secondary protection stage is necessary at CMOS inputs.

## 4 Validation and characterization plan

In order to validate the pad design from functional and ESD point of view, an 8-pin test chip layout is suggested. This chip is expected to be processed as an ordinary chip (sawn, mounted and bonded to a carrier, either Cerdip, PDIP or PCB). For samples intended for ESD stress test, Cerdip or uncoated PCB is recommended to enable post-test failure analysis. The chip schematic and layout is shown below:



Test chip for validation

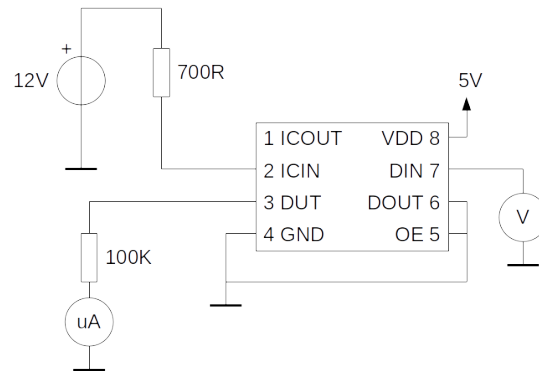
Pins 4 and 8 are the power supply and ground connections, respectively. The **PADGIO** cell of pin 3 is the DUT (device under test) for most of the tests, with all signals accessible. Pads 5,6 and 7 are used to connect to OE, DOUT and DIN signals of the DUT. Pins 1 and 2 are intended solely for the injection coupling test. It is recommended to carry out the tests on as many samples as possible, and process the results statistically.

## 5 Characterization, functional validation

The DUT is intended to perform the functional verification of the design (input, output, tristate functions), and parameter characterization for the most important attributes, like supply voltage range, input levels, output levels under various loads, propagation delays, dynamic power consumption, input capacitance and leakage, output leakage, etc. In order to take into account the changes made to the library and testing concept during development, the actual test specification shall be written after the first samples are available and the scope of validation is defined.

## 6 Injection coupling test

Injection coupling is a parasitic effect in which, when a current is injected into a pin of a chip with a regular pad layout, the leakage of the physically adjacent pins increase significantly. This can occur, for example, when a digital signal is coupled from an off-chip 5V domain into an on-chip 3V domain using a resistor, relying on the parasitic diode of the pin to clamp the voltage. Another situation of concern is in safety-critical automotive applications, where a controlled functional state must be maintained even in the event of a catastrophic failure, that may result in the 12V supply network being coupled to a low-voltage signal on the PCB. This test is intended to verify the susceptibility of the DUT for this condition. The proposed test setup is shown on the figure below:



Scheme of injection coupling test

Pin 3 is set up as an input and it is pulled low via a high resistance (min. 100K). A disturber current of up to 10mA is injected into pin 2, and the level on pin 7 is monitored. The leakage of pin 3 is also monitored. Then, the test is repeated by pulling pin 3 high and injecting negative current into pin 2. It is also recommended to repeat the test with pins 2 and 3 swapping roles. As pass/fail criteria, the level at the DIN signal of the disturbed (non-injected) cell shall not change from the level set by the pullup/pulldown resistor.

## 7 ESD characterization

In order to assess the effectiveness of the ESD protection network, multiple test chips shall be subjected to ESD zapping tests. The target is to reach at least 1KV ESDV rating for HBM. After the zapping tests, units failing under the targeted rating shall be subjected to extensive failure analysis to determine the root cause of the failures, and optimize the ESD design based on the results. In order to take into account the availability of analysis methods and changes made to the library and testing concept during development, the actual test specification shall be written after the first samples are available and the infrastructure to be used for ESD testing and failure analysis is known.

## 8 Further improvements

Currently, the following possible but unaddressed feature additions are considered:

- Schmitt-triggers at input stages
- Switchable weak pullup/pulldown transistors for input and bi-directional pads
- Examine the possibility of locating ESD transistors directly under the bonding pad, thus saving space
- Add level shifters and more sophisticated supply and ESD protection schemes to allow for using multiple voltage domains
- Integrate searling into pad and corner layouts

## 9 References

[1]: Albert Z. H. Wang: On-chip ESD Protection for Integrated Circuits: An IC Design Perspective